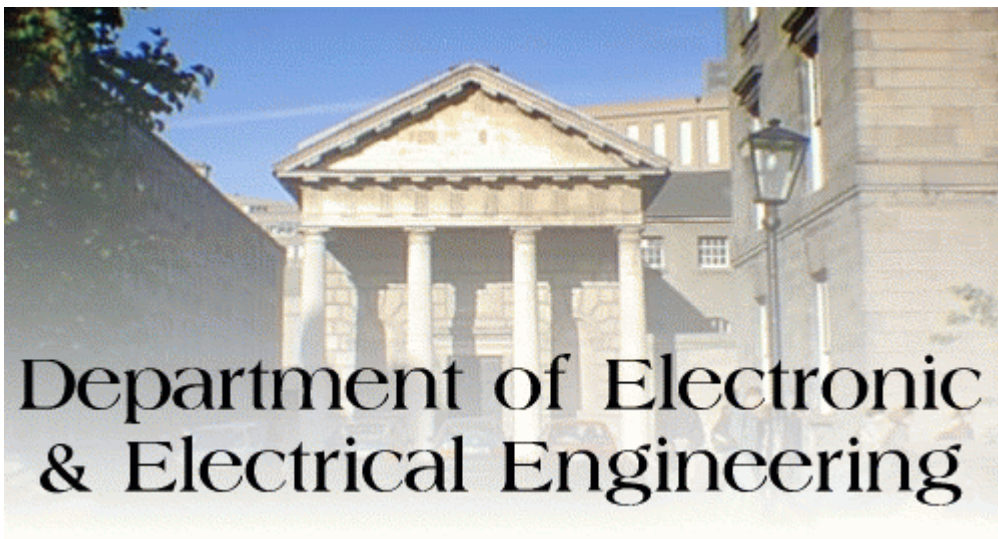


I.C. Technology Processing Course.



Trinity College Dublin

PMOS PROCESS SHEET

Introduction

The object of this course is to provide the student with an opportunity to fabricate a simple PMOS integrated circuit. The chosen circuit contains a transistor, a resistor, a capacitor & two logical devices. The student will acquire an appreciation of some of the fundamental processes of I.C. fabrication. These include oxidation, diffusion, metallisation, lithography and etching.

For the PMOS process, the starting material is an N-type silicon wafer.

Safety Precautions

The following precautions must be observed.

- 1) Everyone in the laboratory must wear a lab coat.
- 2) Heavy duty acid resistant gloves, PVC apron and faceguard must always be worn while working with acids.
- 3) Quartzware must not be touched with bare hands. Sodium from salts on skin causes serious damage to devices & quartzware.
- 4) Students must wear disposable gloves at all times while handling wafers.
- 5) No overcoats, raincoats or food are allowed in the Lab, these may be left in the airlock.

Do not leave valuables in unattended areas.

Some extremely dangerous substances such as hydrofluoric acid (HF) and fuming nitric acid (HNO_3) are used in this Lab. (A pamphlet on the notice board describes the dangers associated with HF). It is therefore imperative for the safety of everyone that due care in the handling of wet chemicals be exercised. In particular, any acid spillages or accidental contact to persons must be reported to the demonstrator immediately. If in doubt about anything **Ask**.

Step 1. Wafer Cleaning:

The wafers are placed in a 1:1 solution of hydrogen peroxide (H_2O_2) and sulphuric acid (H_2SO_4), adding (H_2SO_4) to the (H_2O_2). After about 15 mins a thin surface layer of the silicon is oxidised (less than 10 nm thick). Rinse the wafers thoroughly in de-ionised (D.I.) water.

The thin oxide layer is stripped from the wafer, by dipping it in a dilute solution of HF ($\text{H}_2\text{O}:\text{HF}$, 10:1 vol./vol.) for 10 Secs. This removes any surface contamination. Rinse the wafer, first in the rough rinse bath, then in the Fluoware spray rinser/dryer. The wafer should appear hydrophobic (water should not adhere to the surface). If any droplets remain, this indicates that the wafer is not entirely clean. Repeat step 1 if this occurs. Finally spin dry, using the Fluoware spray rinser/dryer.

Step2. Field Oxidation

Slowly load the wafer into the wet oxidation furnace tube (~30 secs) at a temperature of 1050°C (note each of the six tubes is used for a specific function to prevent "cross-contamination"). While loading the wafer, the tube is purged by passing inert nitrogen gas (N₂) down it.

To start the oxide growth process, the N₂ is replaced by oxygen (O₂) for 5 mins, growing a thin layer of high quality silicon dioxide. (The reason O₂ is used initially is that the surface impurity concentration in the substrate can be altered dramatically when oxidation takes place in water vapour). Next, N₂ is bubbled through a hot water bath (at 98°C) and then to the furnace tube. Now, thermally decomposed steam replaces O₂ as the oxidising agent; the N₂ only being used as a "carrier gas". The wafer is wet-oxidized for 80 mins, after which pure O₂ is switched in for a final 5 mins. This is to provide a high quality oxide at the silicon interface. The oxidised wafer is then withdrawn, in the presence of N₂.

Step 3. Diffusion Masking:

There are 4 masks used in the processing of the simple PMOS I.C. Fig. 1 shows how the 1st mask the diffusion mask is used to define areas of the wafer into which boron will be introduced. Masking, a standard process step, is described in detail below, for this mask. The three other photolithographic masks will be used similarly.

Photolithography:

Photoresist (PR) is now applied to the wafer, which is placed on a horizontally mounted chuck which will be rotated at high speed. First, the static wafer is flooded with the resist, then the excess is spun off, to leave a layer approximately 2 microns (um) thick. The resist spinner setting is 4000 R.P.M. for 30 secs. This method of PR spinning is for fully dehydrated wafers fresh from a drying oven or furnace tube. In the event of wafers with hydrated oxides being used, a layer of adhesion promoter should be applied prior to PR application.

Now, bake the wafer in air at a temperature of 90 – 95°C, for 10- 15 mins. This is called *soft baking* and has the effect of drying solvents out of the two layers. The PR then becomes sufficiently solid to permit careful handling of the wafer, without damage. Next the diffusion mask (Mask 1) pattern is exposed to this thin photosensitive PR layer, using ultraviolet light. The specialized equipment used to apply mask patterns to wafers, is called a mask aligner. The mask, itself is a glass photographic plate on whose emulsion coated side is recorded 100 identical patterns, evenly arranged in a 5 x 20 array. Each pattern is the diffusion mask for one IC- In this way, all array of 100 identical chips are produced on each wafer.

The figures that follow, show only one such die pattern. Also, the sequence of processing operations is illustrated, using the cross-sections of only one of the MOS transistor devices, located on the wafer. Other types of devices on each chip include resistor, capacitor and two logical devices. The mask with emulsion face down is placed on top of and in contact with the wafer and exposed to U.V. light for 42 seconds, using the mask aligner. The wafer is then agitated in an alkaline developer solution for 60 seconds at a temperature of 24- 26°C. The areas exposed to U-V- light are etched away, leaving behind a patterned P.R. layer.

Photolithographic Process with Mask 1

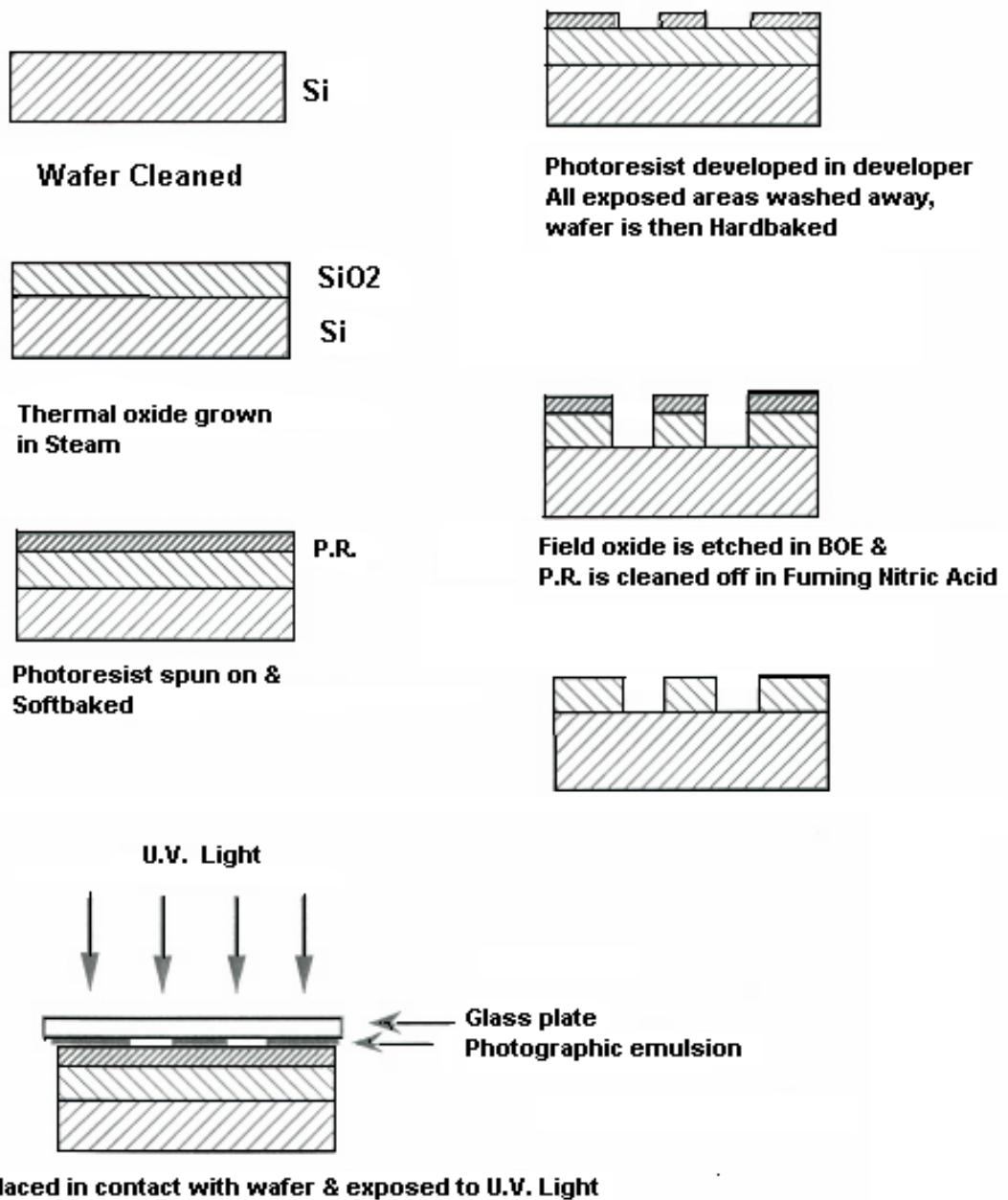


Fig1

Next bake the wafer on a hotplate for 15 mins. at 120 - 125⁰C. This procedure is called *hard baking*. During hard baking, cross-linking of the linear polymer chains in the PR layer occurs, giving a strong 3-D lattice structure. Essentially, this means that the PR becomes acid resistant and difficult to remove without using strong oxidising agents. Obviously, this property allows the PR to be used as a masking layer during chemical etching processes, to provide selectivity in etching.

Step 4. Window Etching:

Etching is carried out to remove exposed blocks of field oxide (i.e., to 'open windows') to reveal the silicon substrate. The wafer is placed in Buffered Oxide Etch (BOE), a HF acid-based solution, at room temperature for 6 mins. This etches away all unprotected silicon dioxide. Following rinsing and drying, the optical microscope may be used to confirm that the oxide has been completely removed in the unprotected regions.

Step 5. Photoresist Removal:

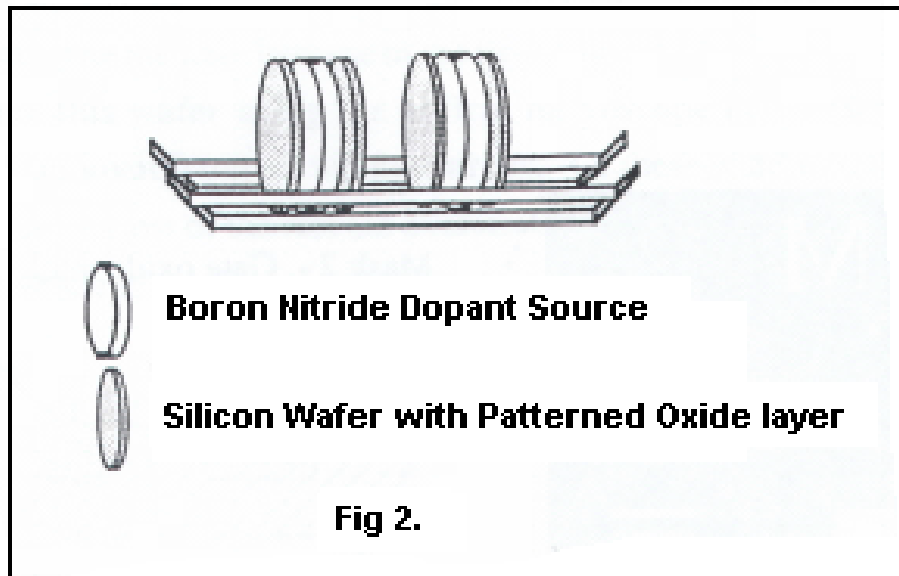
The PR is no longer needed, and is stripped from the wafer by agitation in concentrated fuming nitric acid (HNO₃) for 60 seconds, followed by the cleaning step (Step 1). The patterned oxide layer which remains on the wafer, serves as a mask for "localised well creation", at the boron deposition step.

Step 6. Boron Predeposition :

There are various ways to dope a wafer, such as ion implantation, or by diffusion from gas, liquid or solid dopant sources. In this particular process a solid boron nitride source (BN) is used. For convenient handling in furnace tubes, such solid sources are usually supplied in the same shape as silicon wafers.

The silicon and BN wafers are stacked vertically and close together in a quartz boat (Fig. 2) and slowly loaded into the boron diffusion furnace tube while purging with N₂. Processing time and temperature are 15 minutes and 950⁰C, respectively, in N₂.

The BN source is "activated" with O₂ prior to each lab session to form a surface layer of B₂O₃, this B₂O₃ acts as a local diffusion source. The B₂O₃ migrates at high temperature from the surface of the BN source and diffuses in to the windows opened in the oxide. As the boron diffuses in to the silicon, the oxygen forms an oxide at the surface sealing in the dopant.



Step 7. Boron Drive-In:

As the name suggests, the object of this step is to diffuse the impurity deeper into the substrate, by heat treatment, in the absence of the dopant source. Drive-In is carried out in the wet oxidation furnace at 1050°C in a steam ambient. Process time is 30 mins.

The thin oxide layer in the diffusion windows is thickened in the oxidizing atmosphere. {The regrown oxide is not much thinner than the original field oxide (Fig. 3)}. This facilitates further masking steps and also seals in the impurity. The same processing procedures are used here as in Step 2 (field oxide growth).

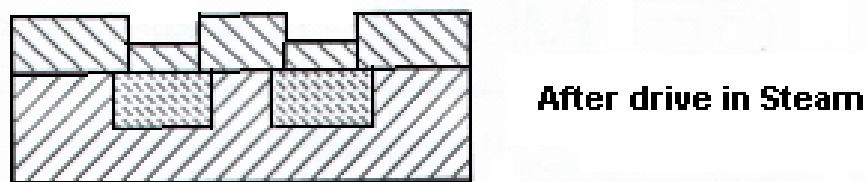


Fig 3.

Step 8. Gate Oxide Mask (first alignment):

Repeat the wafer-cleaning step, then the standard masking and window etching steps (1, 3 and 4) using the gate oxide mask (M2). Since the pattern on this mask plate is being "superimposed" on the existing pattern on the wafer as a result of M1 (Fig. 4), the new pattern must be aligned with the existing one.

The mask aligner is fitted with precision adjustments allowing a wafer to be moved horizontally and rotationally beneath the fixed mask plate. [Successive patterns must

be correctly registered to within 2 μ m accuracy. Alignment markers are provided on each mask plate. The wafer is aligned with successive mask plates by nesting these marks (progressively smaller rectangles and squares) within each other.]

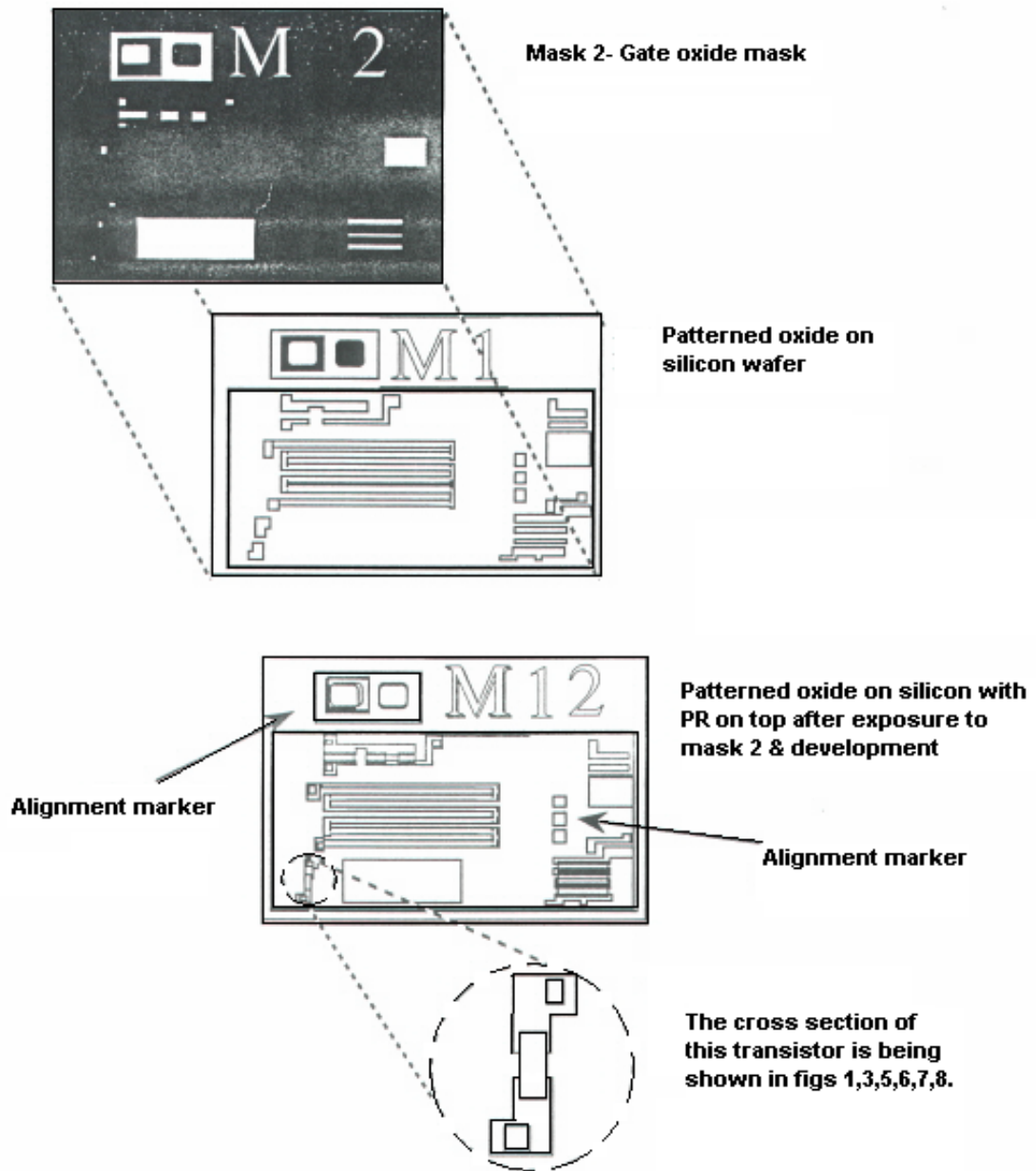
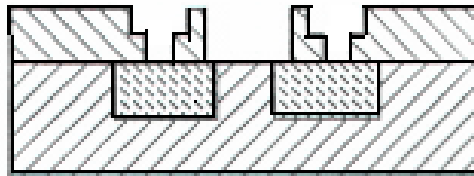


Fig 4.

After masking , the wafer is etched in B.OE for 6 to 10 mins, then spray rinsed and dried(this second oxide etch takes longer than the first, because of the field oxide thickening during drive-in). **It is very important to inspect this wafer using the optical microscope before stripping the resist, to confirm total oxide removal from all window areas.** Of these windows, those astride diffusion regions are gate

regions - most of the rest are oversized contact areas to the diffusion regions (Fig. 5). The latter improve the reliability of subsequent metallisation.



After gate oxide mask

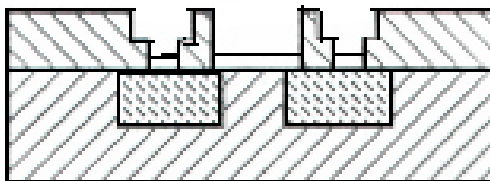
Fig 5.

Step 9. Gate Oxidation:

This is the most crucial processing step since any unwanted impurities in the oxide, eg. Na ions, can cause instabilities in the V_t of the transistors. Trapped charges can also result, depending on the oxidation process parameters. The wafer is loaded into the dry oxidation furnace for 60 mins. at 1050°C in an O_2 ambient (flow $2\text{L} / \text{min}$). A thin uniform layer of high quality oxide is grown in the gate and contact windows (Fig 6). During the process, a little trichloroethylene (TCE) vapour is carried down the tube by a slow bleed of N_2 . The TCE acts as a cleaning agent, or “getter”; thermally dissociated Cl ions are produced, which react with any free alkali ions in the oxide or in the furnace. The salts formed are unreactive. Meanwhile, the ethylene part of the TCE reacts with the O_2 forming CO_2 and H_2O .

Warning: Ensure the O_2 flow always stays above $1\text{L}/\text{min}$ during a process run, otherwise unreacted carbon deposits will form along the tube.

It is normal practice to conclude with an anneal time of around 15 minutes in N_2 to reduce oxide charge. This is less important with PMOS devices and the step is omitted here for speed.



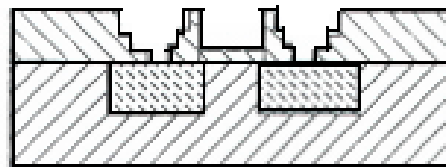
After gate oxide growth

Fig 6

Step 10. Contact-Window Mask (second alignment):

Steps 1, 3 and 4 are repeated here using the contact-hole mask (M3). There are now two patterns on the wafer from masks 1 and 2 and it is becoming more difficult to align. This mask is quite dark and exposure on the aligner should be for 43 secs. Etch

the wafer in BOE for 2 mins. The time is quite short since only a thin gate oxide is being etched (Fig. 7). Confirm the completion of etching using the microscope. Remove the PR from the wafer and apply the cleaning step.



After Contact holes

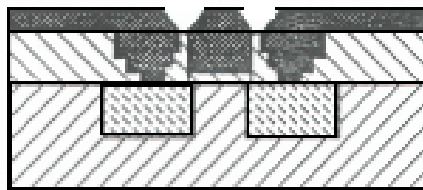
Fig 7.

Step 11. Conductor Deposition:

An aluminium thin film is evaporated onto the wafer surface, ideally of 1 μ m thickness, in a vacuum evaporator using filament or crucible evaporation.

Step 12. Metallization Mask (final alignment):

The metallisation mask (M4) is applied, exposure time is 40 secs and the wafer is etched in orthophosphoric acid (H_3PO_4) to remove unwanted Al. Spray- rinse the wafer, strip the P.R. using fuming HNO_3 ; finish by rough-rinsing and spray rinsing. A pattern of metal tracks remains. These originate from bond pads on the chip perimeter and lead to the various diffusion contacts and gate electrodes (Fig. 8).



After matallisation & pattering with mask 4

Fig 8.

Step 13. Back Contact:

The oxide is removed from the backside of the wafer using BOE, while protecting the active surface of the wafer with a continuous layer of photoresist, which is subsequently removed. Following wafer cleaning, the back of the wafer is coated with Al, and annealed at 450°C for 30 minutes, with an 80% N_2 /20% H_2 gas mixture in the metal annealing furnace tube. This causes alloying at all Al:Si interfaces, assuring good ohmic contacts to the substrate silicon, and is also an effective technique for further reducing oxide charge. The dice on the wafer are now ready for testing.

THE HOT PROBE TEST

NOTE: Gloves are to be worn when handling wafers

1. **AIM:**

To measure the conductivity type of silicon wafers.

2. **APPARATUS:**

2.1 Soldering iron

2.2 Trio digital multimeter (DVM)

3. **METHOD:**

3.1 Plug in the soldering iron and allow it to heat up for several minutes.

3.2 Switch on the DVM.

3.3 Carefully place the test wafer on a flat surface with the tweezers.

3.4 Connect the leads from the soldering iron into the DVM.

3.5 Short the two probes (hot and cold) to zero the DVM.

3.6 Place the two probes on the wafer surface ensuring good contact with the silicon and a reasonable distance between them.

3.7 Note the steady sign on the DVM display.

3.8 Note which wafer you are testing

3.9 Repeat the procedure for the other wafer.

3.10 It is important not to confuse which wafer is which, as it will affect your results for The Four Point Probe Test.

3.11 Turn off all equipment after use and return wafers to containers.

4. **THEORY:**

The Hot Probe Test is a simple way of determining the conductivity type of a silicon wafer. It is based on the fact that by definition a p-type wafer, for instance, has holes as the excess majority carriers. When a hot probe (the tip of a hot soldering iron) is placed in contact with the silicon, energy in the form of heat is imparted to the wafer in that vicinity. The holes absorb this energy and as a result tend to migrate away from the hot site leaving electrons in the majority. Consequently if a voltmeter (DVM) is connected between the two probes a voltage drop will be registered and its polarity will be the opposite to that of the majority carriers. Thus for p-type silicon there will be a negative sign on the DVM. While it is accepted that the mobility of electrons is much greater than the mobility of holes the presence of so many holes is the significant factor. In the case of an n-type wafer a similar argument holds true.

THE FOUR POINT PROBE TEST

NOTE: Gloves are to be worn when handling wafers

1. AIM:

To measure the resistivity of silicon wafers and to determine the dopant concentrations.

2. APPARATUS:

- 2.1 Power supply
- 2.2 Alessi Four Point Probe (FPP)
- 2.3 Trio digital multimeter (DVM)

3. METHOD:

- 3.1 Connect the circuit as shown in Fig. 1. Ensure that the DVM is correctly set and that the power supply is on the 0-1 mA range. The current controller knobs should be in the fully counter-clockwise position.
- 3.2 Switch on the DVM and the power supply.
- 3.3 Carefully place the test wafer on the base-plate of the FPP with a tweezers and slide it under the four probes.
- 3.4 Bring the probes into firm contact with the wafer and lock the arm in the down position (see Fig.2).
- 3.5 Vary the current through the outer two probes with the lefthand knob on the power supply and adjust it to a suitable value (0.4/0.5 mA).
- 3.6 Note the voltage drop across the inner two probes from the DVM.
- 3.7 Record the current (I) and the corresponding voltage (V).
- 3.8 Repeat steps 3.3 - 3.7 at different locations across the wafer.
- 3.9 Calculate the average current (I_{av}) and average voltage (V_{av}).
- 3.10 Calculate the resistivity using the formula: $\rho = 4.532 (V/I) x_j$, where V and I are the average values and x_j is the wafer thickness (= 0.03 cm).
- 3.11 Once the wafer conductivity type has been determined by the Hot Probe Test, the dopant concentration (atoms/cm³) can be read from the graph.
- 3.12 Turn off all equipment after use and return wafers to containers.

4. THEORY

The FPP technique involves passing a fixed, known current between the outermost probes and measuring the corresponding voltage drop across the inner probes. Since the current flowing through the voltmeter is negligible because of its high impedance the contact resistance effects associated with the inner probes is also negligible. Geometric factors such as the probe spacing and sample thickness must be taken into consideration in order to get a reasonable estimate of the resistivity. Depending on the configuration used an appropriate formula is employed.

For this particular set-up $\rho = 4.532 (V/I) x_j$. When the sample is merely bulk silicon, as is the case, x_j represents the wafer thickness. If however, a diffusion had been carried out on the sample then x_j would represent the diffused junction depth. The constant 4.532 is a correction factor to allow for the fact that the current does not flow in a straight line between the outer probes but rather in an arc-like path.

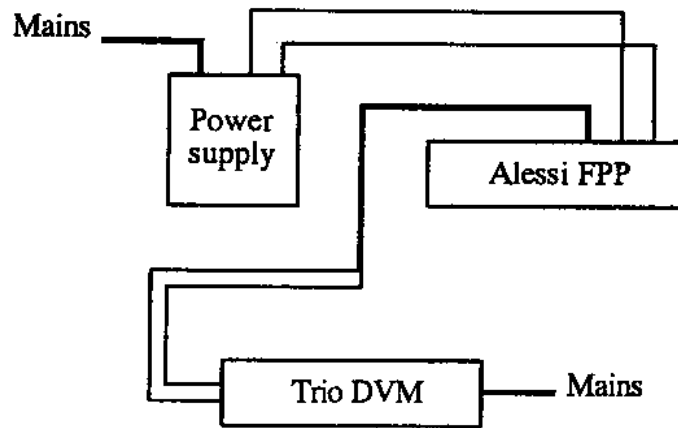


Fig. 1 : Basic circuit for experiment.

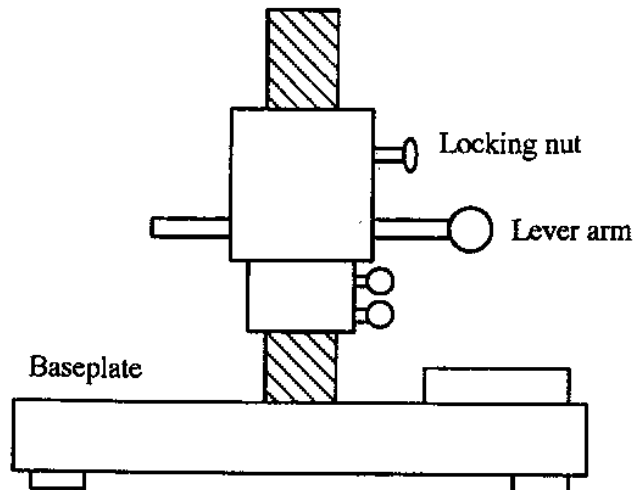


Fig. 2 : Alessi FPP indicating various features.

RESULTS

Name: _____

Group: _____

Date: _____

I(mA)	V(mV)

The average current I_{av} is:

The average voltage V_{av} is:

The wafer conductivity type is:.....

The dopant concentration is:.....

I(mA)	V(mV)

The average current I_{av} is:

The average voltage V_{av} is:

The wafer conductivity type is:.....

The dopant concentration is:.....

DETATCH THIS SHEET AND HAND UP BEFORE LEAVING THE LAB.